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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,557	03/02/2004	Marufa Kaniz	H1248	3296

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EXAMINER
GEE, JASON KAI YIN

ART UNIT	PAPER NUMBER
2434	

NOTIFICATION DATE	DELIVERY MODE
02/05/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing@eschweilerlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/791,557	KANIZ ET AL.	
	Examiner	Art Unit	
	JASON K. GEE	2434	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-10, and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to communication: RCE filed on 07/01/2008 with acknowledgement of filing date of 03/03/2004.

2. Claims 1-5, 7-10, and 19-21 are currently pending in this application. Claim 1 is an independent claim. Claims 19-21 are new.

3. No new IDS was received for this application.

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/09/2009 has been entered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 20, the claim recites two types of separate memory storing different data. The first memory comprises a first memory storing data before encryption and

incoming data after decryption. The second memory comprises storing incoming data prior to decryption and outgoing data after encryption. However, there is overlap of data being stored in the two memories. For example, outgoing data prior to encryption may be the same as incoming data prior to decryption.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 8, 9, 19, and 20 are rejected under 35 U.S.C. 103(a) as being anticipated by Minami et al. US Patent Application Publication 2004/0062267 (hereinafter Minami), in view of Jinzaki US Patent Application Publication 2001/0014936 (hereinafter Jinzaki)

As per claim 1, Minami teaches a network interface system for interfacing a host system with a network to provide outgoing data from the host system to the network and to provide incoming data from the network to the host system, the network interface system comprising: a bus interface system adapted to be coupled with a host bus in the host system and transfer data between the network interface system and the host system (paragraphs 16, 188, 189, Figures 1 and 2), a media access control system adapted to be coupled with the network and to transfer data between the network

interface system and the network (paragraph 16 and throughout the reference; also Figures 1, 2); a memory system coupled with the bus interface system and the media access control system, the memory system being adapted to store incoming and outgoing data being transferred between the network and the host system (paragraphs 1745-1746 and 1765-178, and 1719-1743, wherein the memory is the IPSEC modules; also Figures 66 and 67); a security system coupled with the memory system, the security system being adapted to selectively encrypt outgoing data and to selectively decrypt incoming data (1744-1746 and 1763 to 1766), wherein the security system comprises first and second processors for encrypting the outgoing data_ the first and second processors each being operable independent of one another to encrypt the outgoing data (paragraphs 1744-1746), the security system being configured to send an outgoing data packet to the first processor then a subsequent outgoing data packet to the second processor, then a further subsequent outgoing data packet to the first processor, and continuing in this alternating manner, for encryption (paragraphs 1744-1746).

However, at the time of the invention, Minami does not explicitly teach wherein the processors each comprise pipelines for ESP encryption, ESP authentication, and AH authentication. Minami does teach the use of ESP encryption, ESP authentication, and AH authentication throughout the reference (paragraphs 1744-1746, 105, 896, 1605-1622, and throughout the reference). The use of pipeline processors are well known in the art though, such as seen by Jinzaki in paragraph 222.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the use of pipeline processors. One of ordinary skill in the art would have been motivated to perform such an addition to create more processor power in order to sufficiently support the needs of the process. As seen in paragraph 222 of Jinzaki, pipeline processing becomes necessary when a variety of techniques are required, such as utilizing the ESP encapsulation and tunneling process, along with encryption and decryption needs.

As per claim 2, Minami teaches wherein the two processors are also operable to authenticate the outgoing data (paragraphs 1745-1746).

As per claim 3, Minami teaches wherein the two processors are functionally identical (paragraph 1746).

As per claim 4, Minami does not explicitly teach wherein multiple buffers coupled to the multiple processors. However, this would have been obvious. Buffers are taught throughout Minami, such as in paragraphs 1738, 1748. Even further, buffers are taught all throughout Minami, for example, in paragraphs 219, 221, 223, 509, and much more. Further, Jinzaki teaches the use of buffers throughout the reference, such as in paragraph 184.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement multiple buffers for the multiple processors. As there are two processors both processing data in Minami, which are functionally identical, it would be inherent if not obvious that each processor would have its own input buffer and would be obvious to attach a buffer to each processor, so as to manage the data flow to each

processor. By managing the data flow to the processors, the system can operate more smoothly. Data buffers are known in the art to temporarily store information, and it would be obvious to store data/packets when this data is going to be subsequently used.

Claim 5 is rejected using the same basis of arguments used to reject claim 4 above. Although claim 4 discusses input buffers, output buffers are used in the same way to temporarily store information that is going to be used subsequently, in order to allow the data to flow smoothly.

As per claim 8, Minami teaches wherein the processors comprise pipelines implementing an algorithm selected from the group consisting of the DES-CBC, the 3DES-CBC, and the AES-CBC encryption algorithms (paragraph 1597; also claim 76)

As per claim 9, Minami teaches wherein teh security system further comprises a processor to selectively decrypt incoming data, wherein the security system comprises more than one processor for encrypting and authenticating outgoing data and one processor for decrypting incoming data (paragraphs 1763-1766 and 1744-1746.

As per claim 19, Minamii teaches further comprising a transmit output data flow controller configured to control the flow of encrypted data from the first and second processors to the memory system in the same order as the order in which the data was read from the memory system, such as in paragraph 1746. Further, Janzaki teaches the use of FIFO throughout the reference (paragraphs 94, 96, 137, and 184).

As per claim 20, Minami teaches wherein the memory system comprises: a first memory coupled with the bus interface system and the security system for storage of outgoing dta prior to encryption and incoming data after decryption and a second memory coupled with the media access control system and the security system for storage of incoming data prior to decryption and outgoing data after encryption, wherein the first and second memories comprise different memory locations (paragraphs 1745, 1746, 1764,)

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Minami and Jinzuki as applied above, and in view of Buer US Patent Application Publication 2004/0128553 (hereinafter Buer).

As per claim 7, the Pham combination teaches pipelining throughout Liu, but does not explicitly teach the HMAC-MD5-96 algorithm or the HMACH-SHA-1-96 algorithm. However, Buer teaches this, in paragraph 133.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include the HMAC-MD5-96 or the HMAC-SHA-1-96 algorithm. Both these algorithms are well known in the art, and as the Minami combination is not restrictive on the algorithms used, it would have been obvious to substitute other algorithms for the ones already taught. Further, one of ordinary skill in the art would have been motivated to perform such an addition to improve packet processing techniques and to support secured data transmission over data networks (Buer paragraph 12)

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being obvious over Minami and Jinzuki as applied above, and further in view of Patt, Patel, Evers, Friendly, and Start's "One Billion Transistors, One Uniprocessor, One Chip" (hereinafter Patt).

As per claim 10, Minami seems to propose wherein teh bus interface system, the media access control system, the memory system, and the security system, are included within a single integrated circuit (Figure 1, paragraph 189, and throughout the reference). However, for further clarity, Patt discuses throughout the article that it is well know in the art and would be beneficial to put multiple computing devices onto one chip. For example, this is taught on page 51.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Minami with Patt. One of ordinary skill in the art would have been motivated to perform such an addition to achieve higher performance by keeping latency to a minimum, by locating on the same chip as many as possible of the structures necessary to support a high-performance uniprocessor. Patt teaches this on page 51.

11. Claim 21 is rejected under 35 U.S.C. 103(a) as being obvious over Minami and Jinzaki as applied above, and in view of Chang US Patent No. 5,590,339 (hereinafter Chang)

As per claim 21, the Minami combination does not explicitly teach wherein the memory system comprises a unitary memory system partitioned into first and second

memory areas. However, partitioning memory into separate areas is well known in the art. For example, partitioning memory into different areas for incoming and outgoing data is taught in Chang col. 5 lines 35-43.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the Chang reference with the Minami combination. One of ordinary skill in the art would have been motivated to perform such an addition to control specific types of data and to be able to distinguish and access them. Partitioning memory is very well known in the art, and it also saves expenses as only one hardware memory is needed compared to adding a separate piece of memory hardware.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON K. GEE whose telephone number is (571)272-6431. The examiner can normally be reached on M-F, 7:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on (571) 272-38113811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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